Reliability of InP-Based HBT IC Technology for High-Speed, Low-Power Applications

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***Abstract*— We report on the reliability of an InP-based AlInAs/GaInAs heterojunction bipolar transistor technology which has applications in very high-speed and low power integrated circuits. We have performed extensive accelerated lifetest experiments under different dc bias conditions and different ambient temperatures. For high-performance devices we predict mean-time-to-failures in excess of 10^7 hours at 125°C junction temperatures. We have also investigated the effects of hydrogen on HBT device characteristics which is particularly important for integrated circuits in hermetically sealed packages. We show that the transistor performance is not sensitive to a 4% hydrogen ambient. For integrated circuits requiring precision thin-film resistors we performed lifetest experiments on tantalum-nitride resistors used in our IC process. We show that these thin-film resistors are very stable and exhibit mean-time-to-failures exceeding that of discrete transistors.**

I. Introduction

ALINAS/GAINAS HETEROJUNCTION bipolar transistors (HBT) grown on InP substrates have emerged as a bipolar technology with unique advantages for high-speed, low-power electronics and optoelectronics integrated circuits [1]. From a material standpoint, the InP-based HBT has matured to the level that a wide range of device epitaxial structures and choices of p-type dopants have been reported. The material can also be grown by a variety of epitaxial techniques. The In containing compounds generally exhibit superior electronic properties ideal for bipolar transistors such as low surface recombination velocity, high electron mobility and velocity, and high thermal conductivity of InP substrate. From a device standpoint, InP-based HBT's exhibit millimeter wave RF performance with relatively relaxed material and device designs, have good reliability, are radiation hard, and have low $1/f$ noise characteristics. Furthermore, the low bandgap energy of GaInAs combined with a compositionally graded base-emitter junction results in device turn-on voltages lower than that of silicon bipolar transistors. This translates to a potential for lower IC power dissipation than other bipolar technologies. In addition to unique electronic properties, this technology is compatible with long wavelength photonic devices operating at 1.3 and 1.55 μm. In these applications the base-collector p-i-n photodiode can be readily integrated with the IC technology for multi-Gbps monolithic lightwave receivers.

The AlInAs/GaInAs HBT technology offers a heterojunction bipolar transistor with a GaInAs collector and base layers and an AlInAs emitter layer, both lattice matched to semi-insulating InP substrate. If the base-emitter heterojunction is compositionally graded, the transistor exhibits a turn-on voltage, V_{BE}, less than that of the silicon bipolar transistor with nearly ideal base and collector current characteristics. Using this type of HBT we have demonstrated [2] 39.5 GHz performance of integrated circuits operating at a power supply of 3.0 V. The unique characteristics of the material system also allows us to scale the transistor dimensions to submicron feature sizes while maintaining acceptable dc and rf characteristics. The device scaling is important for reducing IC power consumption. The InP-based HBT technology also offers [3] very stable dc and RF characteristics over a wide temperature range from cryogenics up to 250°C. We have also demonstrated [4] the potential of this technology for microwave power amplification when we incorporated an InP layer instead of the GaInAs for the collector material. An InP collector substantially increases the breakdown voltage to values higher than that of GaAlAs/GaAs HBT. We have previously reported [5] on the reliability performance of InP-based HBT's for low-power operations. We showed that the AlInAs/GaInAs HBT with a compositionally graded base-emitter junction does not exhibit turn-on and dc gain instabilities associated with the base dopant and base-emitter degradations commonly reported for GaAlAs/GaAs HBT's. Since then we have accumulated extensive additional experimental data on alternative device designs and we have examined the effects of hydrogen on discrete InP-based HBT's. With the maturing of the technology, we have also focused on the reliability aspects of integrated circuits which require passive components such as thin-film resistors. For other reliability issues such as metallization which are independent of the technology, we rely primarily on the experience obtained from silicon technologies and from GaAs MESFET technologies.

In general, for low-power, high-speed digital circuit applications of AlInAs/GaInAs technology, a power supply of around 3 V is used. In this application area devices are biased with a collector-emitter voltage, V_{CE} of approximately 1 V and a collector current density of greater than 5×10^4 A/cm^2. For analog circuit applications such as analog-to-digital converters, a power supply of approximately 5 V is used. In this case the devices are biased at a V_{CE} of 2 to 3 V and a collector current density of less than 5×10^4 A/cm^2.

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100 nm	GaInAs Contact	n = 1x10^{19} cm^{-3}
70 nm	AlInAs Emitter Contact	n = 1x10^{19}
120 nm	AlInAs Emitter	n = 8x10^{17}
30 nm	9-Period AlInAs/GaInAs Superlattice Graded Region 23.3 nm n = 8x10^{17} 6.7 nm p = 2x10^{18}	Period 9 (3.3 nm) (3.3 nm) Period 1
10 nm	GaInAs Spacer	p = 2x10^{18}
60 nm	GaInAs Base	p = 2.5x10^{19}
700 nm	GaInAs Collector	n = 5x10^{15}
700 nm	GaInAs Subcollector	n = 1x10^{19}
10 nm	GaInAs Buffer	Undoped
	InP Substrate	

Fig. 1. MBE grown epitaxial profile of the compositionally graded base-emitter AlInAs/GaInAs HBT's.

In this paper, we start with an overview of our HBT material and fabrication process and key device characteristics. Next we will present extensive lifetest data on HBT's stressed at different bias voltages and collector currents pertaining to different applications of the technology. The data presented in this section is obtained from accelerated bias and temperature stress experiments at various ambient temperatures. In this section we will also discuss failure mechanisms, failure criteria and reliability statistics. Next, we report on the effect of hydrogen ambient on InP-based HBT device characteristics which is particularly important for hermetically sealed electronic components. In a hermetically sealed package the part is exposed continuously to an outgassing of hydrogen from the package. Thin film resistors (TFR) are the most critical passive component in an IC process. At the last section we will present lifetest data on tantalum-nitride (TaN) thin-film resistors and compare the reliability of these resistors with discrete devices.

II. Devices and Experiments

The HBT devices used in our experiments were grown lattice matched on InP substrates by MBE. The epitaxial profile for the compositionally graded devices is shown in Fig. 1. The key features include a GaInAs base thickness of approximately 60 nm doped at 2.5×10^{19} cm^{-3} with Be and a GaInAs collector thickness of 700 nm doped at 5×10^{15} cm^{-3} with Si. The devices with a 0.7 μm thick collector compared with our previously reported 0.3 μm collector exhibited a higher device breakdown voltage suitable for circuits operating at a supply voltage of 5 V. With the thicker collector, the RF performance parameters (the unity gain cutoff frequency, f_T and the maximum frequency of oscillations, $f_{\max}$) tend to peak at a current density in the mid 10^4 A/cm^2. The AlInAs emitter was 120 nm thick and doped at 8×10^{17} cm^{-3} with Si. The base-emitter junction was compositionally graded over a distance of 30 nm. This resulted in an average turn-on voltage of 0.65 V for a number of devices at the lifetest bias condition ($V_{\rm CE} = 3.0$ V and $J_C = 2.5 \times 10^4$ A/cm^2.

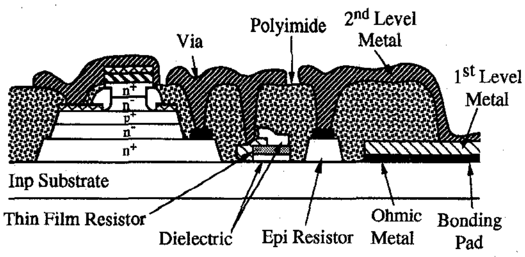

Fig. 2. Schematic cross section of a triple-mesa, planarized HBT along with thin-film resistor.

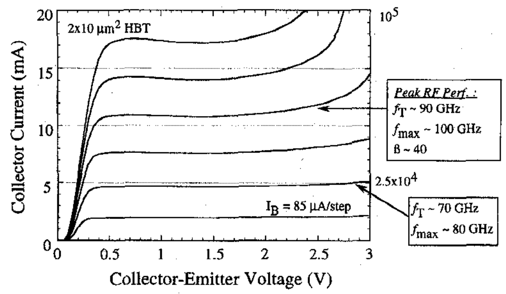

Fig. 3. Measured IV characteristics of typical InP-based HBT's. RF performance is also shown at different biases.

Devices were fabricated using our triple-mesa process [6] to access the base and collector and to isolate the device. Non-alloyed Ti/Pt/Au was used for the emitter and base ohmic contacts and AuGe/Ni/Au for the collector contacts. Subsequently, thin-film resistors (TFR) and metal-insulator-metal (MIM) capacitors were fabricated on the substrate. Tantalum nitride (TaN) TFR's were confined within two layers of silicon nitride which enhances the long-term stability of these resistors. The mesa structure resulting from the device fabrication was planarized by polyimide which was then etched back by reactive ion etching (RIE) to expose the emitter tops. Via holes were subsequently etched in the polyimide using RIE to reach the base and collector and the resistor and capacitor terminals. The second level of metallization was patterned over the polyimide for interconnection. The schematic cross-section of a planarized HBT with resistors is shown in Fig. 2.

The I_C-$V_{\rm CE}$ characteristics of a typical HBT with a 0.7 μm thick collector are shown in Fig. 3. At peak RF performance, the f_T and $f_{\max}$ of this device was 90 and 100 GHz, respectively. The dc current gain was 40. The collector-emitter breakdown voltage of this device is dependent on the collector current. At a current density of 2.5×10^4 A/cm^2 the breakdown voltage is approximately 4.5 V so the device can be safely operated at a 3 V bias. The RF parameters and dc current gain of a device with a 0.3 μm thick collector is shown in Fig. 4. The f_T of this device peaks to a value of 130 GHz while the $f_{\max}$ is lower than f_T due to the higher base-collector capacitance associated with the thin collector design. The breakdown voltage of this device is lower and is generally biased at a collector-emitter voltage of about 1.0 V and a collector current density of greater than 5×10^4 A/cm^2.

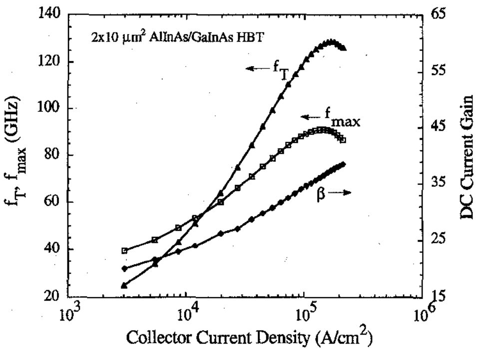

Fig. 4. f_T, $f_{\max}$, and dc current gain as a function of the collector current density for a 2×10 μm^2 HBT with 0.3 μm thick collector.

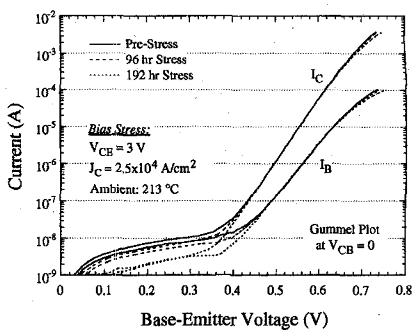

Fig. 5. Measured base and collector currents as a function of base-emitter voltage shown before and after stress for a 2×3 μm^2 HBT.

To determine the reliability of InP-based HBT devices for IC applications we have performed accelerated lifetest experiments at elevated temperatures ranging from 193°C to 228°C ambient temperatures. Since device degradation and failure modes are strongly dependent on dc bias conditions, for reliability evaluations discrete devices were held under a constant dc bias. We stressed two types of devices. The first group was designed for low-voltage, and low-power digital IC applications with a collector thickness of 0.3 μm and exhibited a f_T of 130 to 140 GHz. In our lifetest experiments these devices were stressed at $V_{\rm CE} = 1.0$ V and collector current density, $J_C = 7 \times 10^4$ A/cm^2. The second group of devices were biased with $V_{\rm CE} = 3.0$ V and $J_C = 2.5 \times 10^4$ A/cm^2 (for analog and precision ADC applications).

To perform accelerated lifetesting, discrete devices with a substrate thickness of 100 μm were packaged. The transistors were biased in the forward active mode with a constant current density and a constant collector voltage. DC bias was applied to the devices at room temperature, then the oven temperature was raised to the desired level. Initial device characterization and subsequent periodic monitoring of device characteristics was performed at room temperature. We performed extensive dc characterization periodically during the lifetest (at room temperature) which included Gummel and I_C-$V_{\rm CE}$ measurements and base-emitter (B-E) and base-collector (B-C) junction characteristics both in the forward and reverse modes. $V_{\rm BE}$ was measured at a low current density to monitor the stability of the turn-on voltage. $V_{\rm CE}$ offset voltage and junction leakage currents were also recorded to monitor the stability of the B-E and B-C junctions. Junction temperature rise under applied bias and device thermal resistance were measured directly using the liquid crystal technique. Using this technique we obtained a thermal resistance of 4.72°C/mW/μm^2 for a device with an emitter geometry of 2×3 μm^2.

The areas of reliability concern in bipolar transistors is generally the stability of junctions, ohmic contacts, and dc current gain. Of particular importance in GaAs-based HBT's is the stability of the base-emitter junction and the dc current gain. In Be-doped GaAs-based HBT's under applied bias, the Be diffuses from the base into the base-emitter junction and leads to instability in the turn-on voltage and dc current gain [7]. In carbon-doped GaAs HBT's the dc current gain and B-E junction degrades due to a strain in the base [8]. Our extensive lifetest data on AlInAs/GaInAs HBT's with graded base-emitter junctions indicate that no such degradation exists in these devices. This is evident from the dc measurements taken before and after stress and are shown in the following section. Another important area of reliability concern is the effect of exposure to hydrogen on device characteristics. In hermetically sealed packages, hydrogen outgasses continuously from the package and has been shown to degrade HEMT's [9] and GaAs/AlGaAs HBT's [10]. In the case of GaAs HBT's the H_2 interacts with the base dopant and causes instability in the dc current gain. The degradation is rapid and can take place in a few hundred hours even at low ambient temperatures. To examine the effect of hydrogen on InP-based HBT's, we exposed these devices to a 4% H_2 ambient for a stress period of over 300 hours at 200°C. During this test, dc bias was also continuously applied to the devices under stress ($V_{\rm CE} = 3$ V, $J_C = 2.5 \times 10^4$ A/cm^2).

III. Experimental Results and Discussion

A. HBT Lifetests

In this section, we examine some of the key dc current-voltage characteristics and device parameters pertinent to the reliability assessment of InP-based HBT's. In particular, we pay close attention to the stability of the two junctions of the bipolar transistors. For the B-E junction stability, the measurements of base and collector currents as a function of the turn-on voltage taken before and after stress is shown in Fig. 5. This figure is the Gummel plot of base and collector currents before stress, after 96 hours, and after 192 hours of stress at 213°C. The measurements shown in Fig. 5 indicate there is stability in the dc current gain, turn-on voltage, and B-E junction characteristics. In addition, the plot also indicates that the contact resistances are unaffected by the bias and thermal stress. This is evident from the region of the measurement at high values of current where the effect of series resistances is more profound. The I-V measurements of Fig. 5 demonstrate the stability of emitter, base, and base-emitter junction of these InP-based HBT. Stability of the turn-on voltage, $V_{\rm BE}$ is crucial in the bipolar transistors, particularly for analog circuit applications. We monitored the intrinsic turn-on voltage of the devices during the stress period

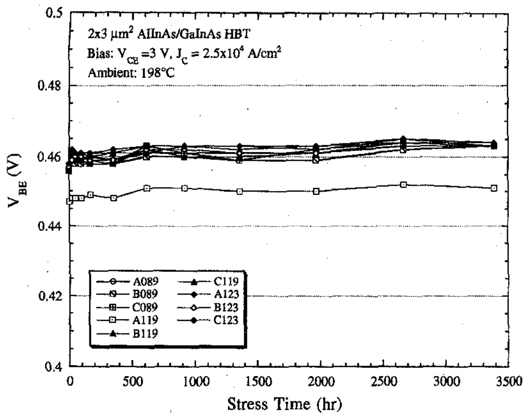

Fig. 6. Base-emitter turn-on voltage measured at 5 A/cm^2 collector current density as a function of stress time at 198°C ambient.

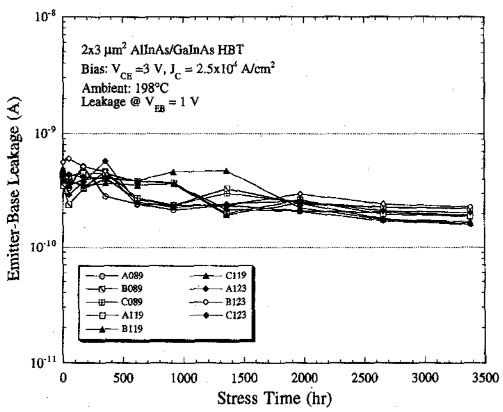

Fig. 7. Emitter-base reverse-biased leakage current measured at $V_{\mathrm{EB}} = 1$ V as a function of stress time at 198°C ambient.

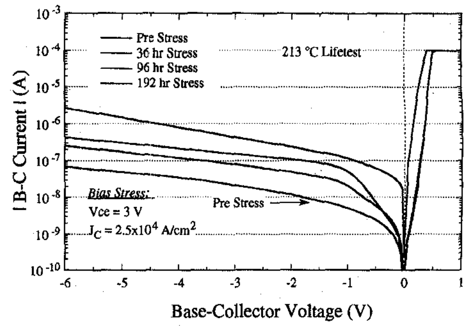

Fig. 8. Measured I-V characteristics of InP-based HBT under bias and temperature stress, showing gradual increase in the B-C junction leakage current.

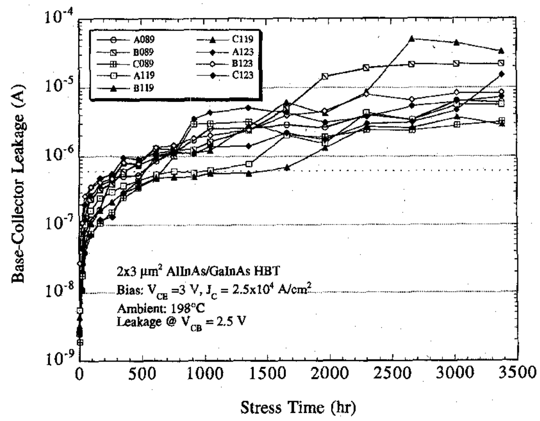

Fig. 9. Base-collector reverse-biased leakage current measured at $V_{\mathrm{CB}} =$ 2.5 V as a function of stress time at 198°C ambient.

by measuring the V_{BE} at a low collector current to avoid the effect of series resistances. This is shown in Fig. 6 for 9 devices over a stress period of 3400 hours at an ambient temperature of 198°C. Similarly, the base-emitter leakage current was monitored over the same stress period. The leakage was measured at a reverse bias of -1.0 V. The measured data for 9 devices is shown in Fig. 7 which indicates that the leakage current gradually *decreases* with increasing stress time.

Fig. 8 is a plot of the base-collector junction characteristics under bias stress which shows a gradual increase in the base-collector (B-C) leakage current under stress. This device was stressed in ambient of 213°C with a bias of 3 V. The rate of increase in the leakage current is dependent on the peak electric field at the B-C junction and the amount of stress current. Therefore, varying the bias voltage or the thickness of the collector affects the rate of degradation which is caused by hot electrons generated at the peak electric field. Base-collector leakage current for individual devices was measured at a reverse bias of -2.5 V which is approximately equal to the reverse bias of a transistor with a 3.0 V V_{CE} bias voltage. The increase in the B-C leakage current over a stress period of 3400 hours is shown in Fig. 9 which was performed at an ambient temperature of 198°C. The plot indicates an initial rapid increase in the reverse leakage current of the B-C junction followed by a long period where the leakage increase is gradually leveling off. The initial stage of rapid change can be included in a burn-in or stabilization period normally applied prior to delivery of parts. We have used the increase in the base-collector leakage current to set a failure criteria for assessing the useful life of this technology for integrated circuit applications.

Under normal operating conditions the B-C leakage current is injected from the collector to the base thus canceling the base current and causing the current gain to appear higher. For circuit performance, the leakage current must remain small compared to the collector current while the apparent increase in the current gain dose not affect the circuit performance. However, as a conservative failure criterion we required that the leakage current remain less than a fraction of the base current. Applying this criterion to the data taken periodically throughout the lifetest such as that shown in Fig. 9, we can obtain a time-to-failure corresponding to a cumulative number of devices that failed. Such a plot is shown in Fig. 10 for data obtained at 3 different ambient temperatures using a log scale for the time-to-failure and a normal probability distribution scale for the cumulative failure as a percentage of the total test population. A linear least-square fit to this data is also shown in Fig. 10 which is an indication that the failures fall into a lognormal probability distribution , with an associated

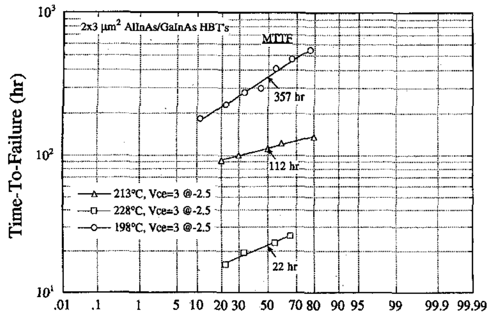

Fig. 10. Log normal plot of time-to-failure of HBT's as a function of cumulative failure for 3 ambient temperatures of 198, 213, and 228°C.

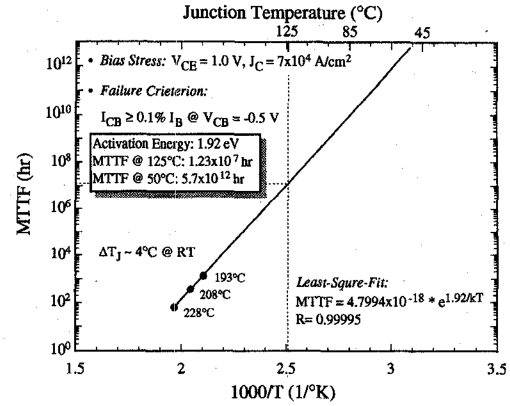

Fig. 11. Arrhenius plot of MTTF for devices with 1.0 V bias stress for low-voltage, low-power digital IC applications.

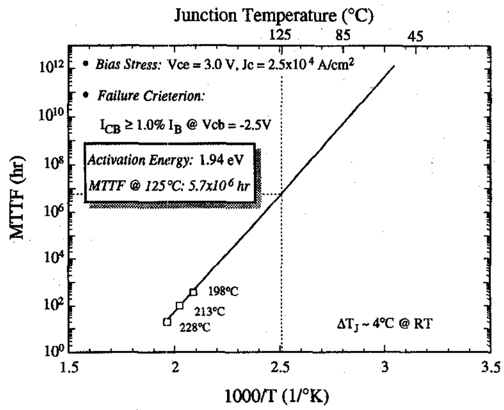

Fig. 12. Arrhenius plot of MTTF for devices with 3.0 V bias stress for analog IC applications.

σ (dispersion or shape factor) of about 0.5. The σ is estimated as ln(time-to-50% failure) minus ln(time-to-16% failure). A lognormal distribution is commonly encountered in solid-state device failures [11] and the associated σ strongly affects the failure rate.

From the plots of time-to-failure such as shown in Fig. 10, we obtain the mean-time-to-failure (MTTF) corresponding to a cumulative failure of 50 percent. we can project the useful device life using an Arrhenius plot of the MTTF as a function of ambient temperature such as the plot shown in Fig. 11. In this plot, each of the three data points (corresponding to three different ambient temperatures) represents the mean-time-to-failure of a sample device population stressed at $V_{CE} = 1$ V and $J_C = 7 \times 10^4$ A/cm^2. This is our stress condition for low-voltage, low-power applications of the technology. The Arrhenius plot of the data projects a MTTF of 1.23×10^7 hours at 125°C ambient. The activation energy for the B-C junction degradation mechanism is estimated from the figure to be 1.92 eV. Similarly, lifetests were conducted for devices which were biased with $V_{CE} = 3$ V for IC applications requiring a 5.0 V power supply. The Arrhenius plot of Fig. 12 summarizes the results of the three lifetest experiments at ambient temperatures of 198, 213, and 228°C. At this bias condition, the activation energy was the same as before. The projected MTTF at 125°C ambient was 5.7×10^6 hours. Having determined the MTTF and the sigma of the lognormal distribution, we can estimate the failure rate, λ which is expressed in failure unit (FIT) defined as 1 failure in 10^9 hours of device operation. To determine the total number of failures in an interval of device operation, we can then multiply the failure rate by the particular time interval. Failure rate can be estimated from the following equation from Jordan [12]

$$\lambda(t) = \frac{\sqrt{2}\exp\left[-\frac{1}{2\sigma^2}\left(\ln(t/t_m)\right)^2\right]}{\sqrt{\pi}\, t\, \sigma\, \mathrm{erfc}\frac{1}{\sqrt{2\sigma}}\ln(t/t_m)} \times 10^9.$$

Where σ is the lognormal dispersion or shape factor, t is operating time, t_m is the MTTF at operating temperature, and λ is the failure rate in unit of FIT. For example for a $\sigma = 0.5$, $t_m = 10^7$ hr, $t = 10^5$ hr (approximately 11.5 years of operation), the λ from the above equation is 3×10^{-15} FIT. To show the importance of σ, for the same example, a σ of 3 yields a failure rate of 407 FIT.

B. Effect of Hydrogen on HBT's

Effect of hydrogen on compound semiconductor devices such as HEMT [9] and GaAs/AlGaAs HBT [10] have been reported previously. For GaAs/AlGaAs HBT's with a carbon-doped base layer it has been reported that the hydrogen, perhaps in its elemental form, interacts with the base dopants and causes instability in the dc current gain of devices after a short period of exposure to hydrogen. To examine the effect of hydrogen on InP-based HBT's we performed a lifetest at 200°C and 4% H_2 ambient with a bias condition of $V_{CE} =$ 3 V and $J_C = 2.5 \times 10^4$ A/cm^2 which is the bias condition used in one of our previously discussed lifetests. A number of devices were included in this experiment including control samples which were not exposed to the 4% hydrogen. Devices were characterized periodically at room temperature. Fig. 13 shows the comparison of dc current gain of devices with and without exposure to the 4% H_2 ambient. We did not observe any effect specifically due to exposure to hydrogen in these devices.

C. Thin-Film Resistors

Thin-film resistors are the most critical passive component in integrated circuit processes. In our HBT IC process we fabricate TFR's by patterning a film of 80 nm thick sputtered

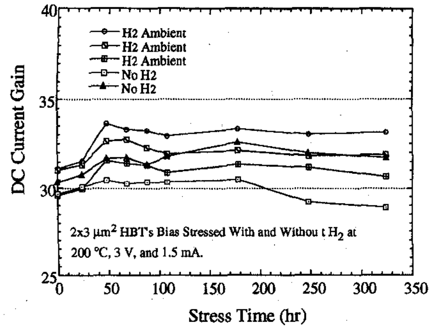

Fig. 13. DC current gain of HBT's bias stressed with and without exposure to hydrogen.

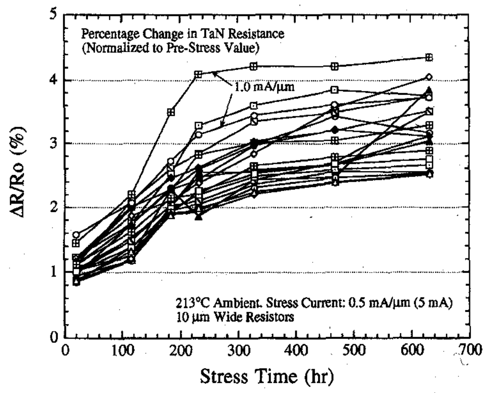

Fig. 14. Relative change in the resistance of 100 Ω TaN thin-film resistors bias stressed at 213°C ambient with two different stress currents.

TaN. The film which is deposited on a layer of silicon nitride provides a sheet resistance of 50 Ω/sq. The TaN film is reactive ion etched for precise definition and size control. We did extensive lifetests on TaN resistors (fabricated along with HBT's in the IC process) under bias and temperature stress. The individual resistors were packaged and biased with a constant current of either 0.5 or 1.0 mA/mm corresponding to 5 mA of current through a 10 μm or a 5 μm wide resistor, respectively. The lifetests were performed at 213°C and 228°C and resistor values were monitored periodically during the lifetest at room temperature. Fig. 14 shows the relative change in the resistance of typical 100 Ω resistors biased with two different current densities at a 213°C ambient. The same data taken at lifetest of 228°C ambient with 0.5 mA/mm and 1.0 mA/mm of constant current is shown in Figs. 15 and 16, respectively. In each case, the change in resistor value is gradual and tend to saturate with increasing stress time. For integrated circuit applications we can tolerate a 2% change in the value of thin film resistors. Based on this tolerance we define a "failure criterion" of 2% for $\Delta R/R_0$, where R_0 is the as processed resistor value. The mean-time-to-failure of resistors is obtained from the lognormal plot of Fig. 17 for ambient temperatures of 213°C and 228°C. We notice that for either of the two temperatures, the MTTF of thin-film resistors is greater than that of our HBT's at same stress temperatures. Furthermore, the sigma (shape factor) of resistor failure distribution is comparable with that of the transistors.

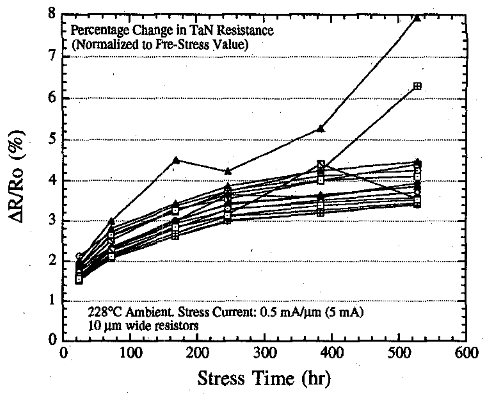

Fig. 15. Relative change in the resistance of 10 μm wide 100 Ω TaN thin-film resistors bias stressed at 228°C ambient with a stress current of 0.5 mA/mm.

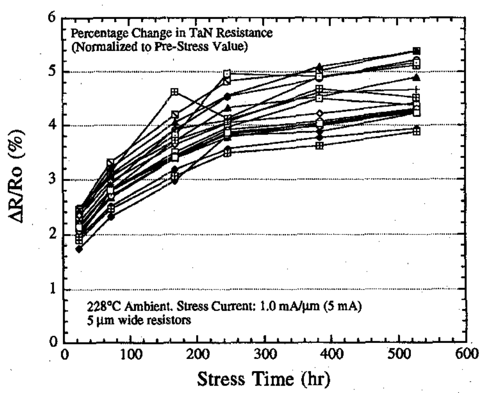

Fig. 16. Relative change in the resistance of 10 μm wide 100 Ω TaN thin-film resistors bias stressed at 228°C ambient with a stress current of 1.0 mA/mm.

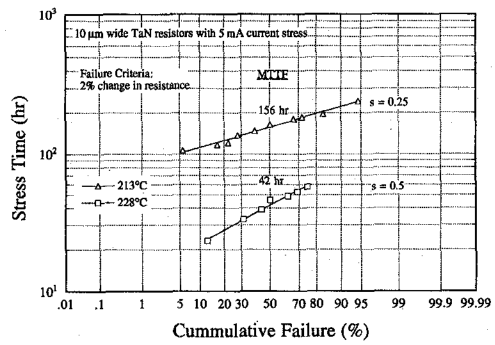

Fig. 17. Log normal plot of time-to-failure of TaN resistors as a function of cumulative failure for two ambient temperatures of 213°C, and 228°C.

Based on this data we conclude that the resistor reliability exceeds our IC requirements.

IV. Summary and Conclusion

We have conducted a systematic and extensive characterization of an HBT IC technology with millimeter wave performance. Our AlInAs/GaInAs HBT's are free from base dopant related instabilities observed in GaAs-based HBT's which lead to drift in turn-on voltage and dc current gain. AlInAs/GaInAs HBT's are also insensitive to hydrogen which is encountered in applications requiring hermetically sealed packaging of electronic components. Tantalum-nitride thin-film resistors in our IC process exhibited mean-time-to-failures exceeding that of active devices. These precision resistors exceed the tolerance requirements of our integrated circuits. Our reliability results indicate that this technology has tremendous potential for high-performance, low-power applications with stringent reliability performance requirements.

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